DEVELOPMENT OF VOLTAGE-CONTROLLED SAW OSCILLATOR (VCSO) FOR FIBER-OPTIC COMMUNICATION SYSTEMS

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ABSTRACT

Oscillators based on the SAW (surface acoustic wave) technology in general offer lower noise compared to the conventional crystal oscillators at higher frequencies. VCSO (voltage-controlled SAW oscillator) can be an important component in the phase lock loop (PLL) subsystem for clock and data recovery (CDR), clock smoothing or frequency translation in the SONET/SDH (Synchronous Optical Network / Synchronous Digital Hierarchy) fiber-optic communication systems. In this paper, the developing procedures and test results for a 622.08 MHz VCSO are recorded. The test results include the waveform, variation of frequency over control voltage range, and phase noise. The pulling range, frequency-voltage linearity and phase jitter measured for the first prototypes are +170 ppm/-190 ppm, 12 % and 0.17 pSec, respectively.

Keywords: VCSO, SAW, pulling range, linearity, waveform, phase noise, phase jitter

I. INTRODUCTION

Nowadays, the operations of clock and data recovery (CDR), clock smoothing or frequency translation of fiber-optic communication systems such as the SONET/SDH (Synchronous Optical Network / Synchronous Digital Hierarchy), are provided by voltage-tunable high frequency clock sources with, absolute pulling range exceeding ±50 ppm in an operating temperature range of -40 to 85 ^{O}C, frequency-voltage linearity smaller than 15%, and phase jitter less than 1 pSec integrated from 12 KHz to 20 MHz of the offset frequency from the carrier.[1,2]

A voltage-controlled crystal oscillator (VCXO) is good for clocking up to about 100 MHz. For higher frequencies, surface acoustic wave (SAW) device is often used in the resonant circuit instead of a crystal. SAW components are used extensively in supporting frequency generation and control of modern telecommunication systems. Oscillators based on the SAW technology in general offer lower noise compared to the conventional crystal oscillators at higher frequencies. For crystal to meet the requirements at high frequencies, expensive high fundamental frequency (HFF) crystal blanks are required. Multiplication stages can be used to achieve higher frequencies but the phase noise of the oscillator degrades with by a factor of 20 log N, where N is the multiplication factor.[3]

The purpose of this paper is to develop a 622.08 MHz voltage control SAW oscillator (VCSO) for SONET/SDH timing applications. It also can be used in phase lock loop (PLL) applications for clock smoothing and frequency translation. Testing results, including of the pulling range, linearity, phase noise, phase jitter and waveform are included.

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II. SAW RESONATOR

SAW is an acoustic wave propagating along the surface of piezoelectric substrates and the amplitude decays exponentially with substrate depth. SAW can be generated and detected by metallic interdigital transducer (IDT) on a piezoelectric substrate and the frequency is calculated by equation (1).

$$f = V / \lambda \qquad (1),$$

where

V : SAW velocity

λ : Period of IDT

In case of using ST-cut quartz as the piezoelectric substrate, the velocity of the SAW is about 3100 m/s. The 1-port SAW resonator (SAWR) consists of two reflective gratings and an IDT between them. The IDT is used to excite and detect the standing SAW that builds up between the reflective gratings. This construction provides a high quality factor resonator.[4] As shown in figure 1, the equivalent circuit near resonant for such a 1-port SAWR has series resonant arm containing the motional elements C_m, L_m, and R_m shunted by a static capacitance C_o of the IDT. The C_m, L_m, R_m and C_o of the SAWR we used are 1.73 fF, 37.8 uH, 18 Ohm and 2.18 pF, respectively.

III. PIERCE-TYPE OSCILLATOR

The Pierce-type oscillator circuit of the VCSO is shown in figure 2. The capacitor at the base-to-GND and capacitor at the collector-GND along with the SAW resonator, which acts as an inductor, form a pi-network to provide the required phase shift so to fulfill the Barkhausen's oscillation criteria. From another viewpoint, oscillation can be sustained because the capacitor C_1, together with the C_2 and the transistor, provides the negative resistance (gain) which cancels with the loss due to resistance of the resonator. C_1 and C_2 affect the center frequency and the frequency tuning bandwidth. The inductance L_1 can drag the load capacitance into the inductive domain such that frequency control range can be widened. In other words, the separation between the resonating frequency and anti-resonating frequency will increase when an inductor is added in series with the SAW resonator. Through this, the pulling range of the VCSO can be increased. By changing the load capacitance of the oscillation circuit with the characteristic of capacitance versus reverse direction voltage of the varactor diode D_1 (varicap), one can change the output frequency. The SAWR, L_1 and D_1 together act as an effective resonator whose reactance can be changed by the control voltage. R_1 is a shunt feedback resistor from the collector to base for adjusting the feedback power into the effective resonator. The supply voltage for the VCSO is 3.3 V instead of the conventional 5.0 V so to achieve lower power consumption and faster signal processing. The VCSO circuit was designed with fast startup, guaranteed oscillation and good phase noise such that the relationship between the negative resistance, R_N, and R_m satisfies equation (2) at startup oscillation.

$$\left|R_N\right| > 5 \times Rm \qquad (2)$$

The negative resistance from 600 to 700 MHz is shown in figure 3. The negative resistance is 130 Ohm at 622.08 MHz and so it is practical for the SAWR we used.

IV. TESTING RESULTS

The variation of the output frequency for the prototype 622.08 MHz VCSO with control voltage from 0.3 to 3.0 V with a 0.15 V step is as shown in figure 4. The center value of the control voltage is 1.65 V, which is the half value of the supply voltage. The frequency increases with the increase of the control voltage and puling range is about +200 ppm/-240 ppm. The generally accepted definition of linearity is the ratio between frequency error and total deviation, expressed in percent, where frequency error is the maximum frequency excursion from the best straight line fit. The linearity calculated is 11.5 %. The waveform of the VCSO is measured with a scope of 6 GHz bandwidth. The output is a differential LVDS logic and the waveform is measured at the center control voltage of 1.65 V, as shown in figure 5. The rise/fall time, voltage swing and duty cycle are about 370 pSec, 750 mV and 49 %, respectively. The phase noise of the 622.08 MHz VCSO is measured with the three components comparison method using an Agilent phase noise testset. As seen from figure 6, the phase noise is -70, -100, -130 and -140 dBc/Hz at 100 Hz, 1 KHz, 10 KHz and 100 KHz offset from the carrier, respectively. Figure 7 shows the phase noise from 12 KHz to 20 MHz. The phase jitter can be calculated by using equation (3) which involves the integration the phase noise result from 12 KHz to 20 MHz:

$$\text{RMS Jitter in seconds} = \frac{(360/2/3.14) \times 10^{(\text{Value of definite integral}/20)}}{360 \times \text{Frequency}}$$

The calculated phase jitter is about 0.17 pSec which meets comfortably the SONET requirement of smaller than 1 pSec.

V. CONCLUSION

This study is to develop a 622.08 MHz VCSO for the fiber-optic communication systems. The pulling range achieved is about +200 ppm/-240 ppm with an inductor in series with a 1-port SAWR and a varicap in a Pierce-type oscillator. The linearity is about 12 % with the control voltage range from 0.3 to 3.0 V. The phase jitter is 0.17 pSec in the frequency range from 12 KHz to 20 MHz.

References

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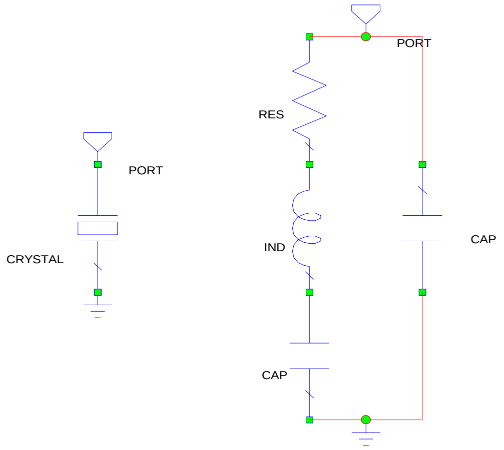


Figure 1. Equivalent Circuit of 1-port SAWR.

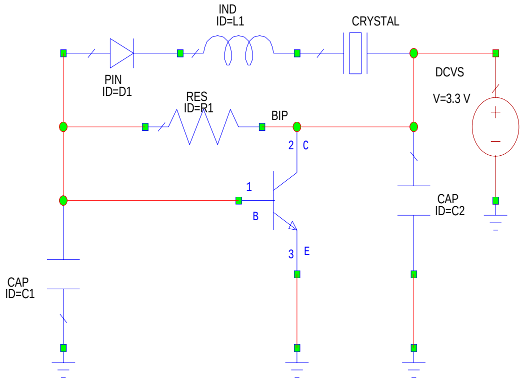


Figure 2. Basic circuit of the Pierce type VCSO.

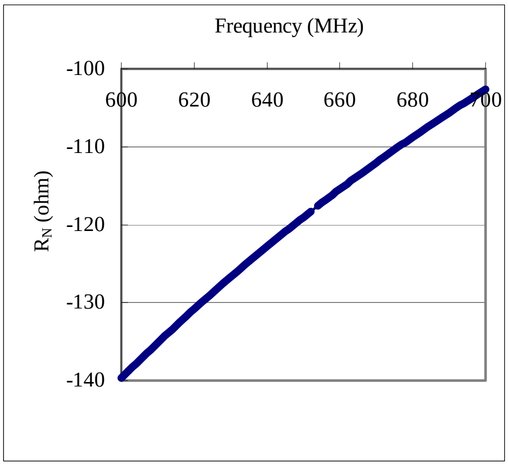


Figure 3. Negative Resistance from 600 to 700 MHz.

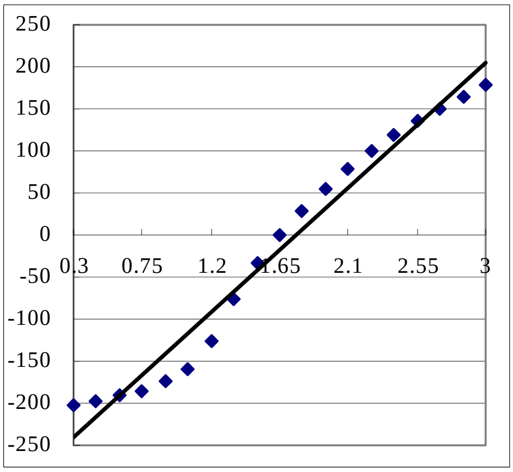
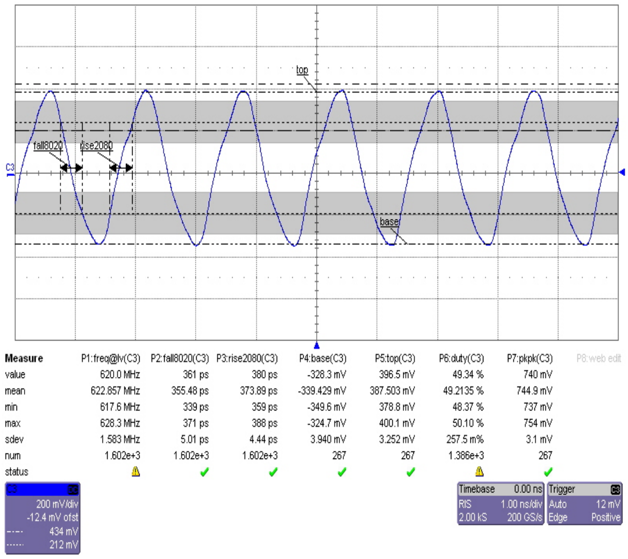


Figure 4. Variation of the Output Frequency with Control Voltage.



Measure	P1:freq@lv(C3)	P2:fall8020(C3)	P3:rise2080(C3)	P4:base(C3)	P5:top(C3)	P6:duty(C3)	P7:pkpk(C3)	P8:web edit
value	620.0 MHz	361 ps	380 ps	-328.3 mV	396.5 mV	49.34 %	740 mV	
mean	622.857 MHz	355.48 ps	373.89 ps	-339.429 mV	387.503 mV	49.2135 %	744.9 mV	
min	617.6 MHz	339 ps	359 ps	-349.6 mV	378.8 mV	48.37 %	737 mV	
max	628.3 MHz	371 ps	388 ps	-324.7 mV	400.1 mV	50.10 %	754 mV	
sdev	1.583 MHz	5.01 ps	4.44 ps	3.940 mV	3.252 mV	257.5 m%	3.1 mV	
num	1.602e+3	1.602e+3	1.602e+3	267	267	1.386e+3	267	
status	⚠	✓	✓	✓	✓	⚠	✓	

C3 DC
200 mV/div
-12.4 mV ofst
434 mV
212 mV

Timebase 0.00 ns
RIS 1.00 ns/div
2.00 kS 200 GS/s

Trigger C3
Auto 12 mV
Edge Positive

Figure 5. Waveform of the 622.08 MHz VCSO at Center Control Voltage.

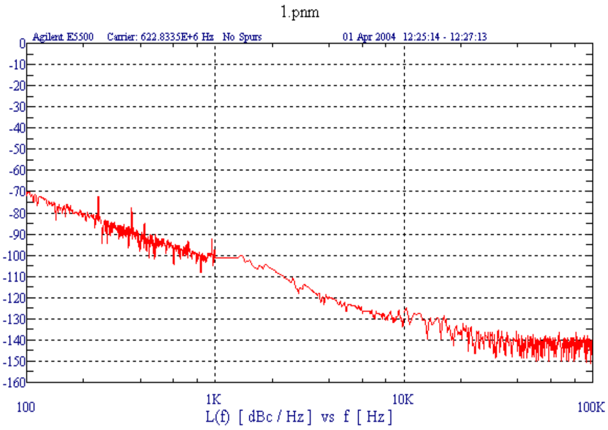


Figure 6. Phase Noise of the 622.08 MHz VCSO from 100 Hz to 100 KHz.

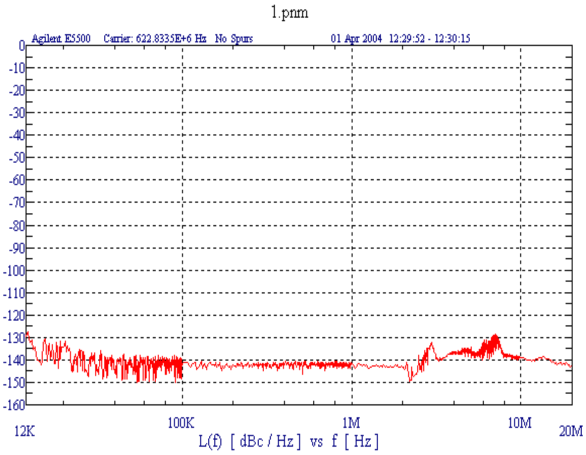


Figure 7. Phase Noise of the 622.08 MHz VCSO from 12 KHz to 20 MHz.